ECC UDIMM
DDR5 5600 48GB
Datasheet

(SQR-UD5N48G5K6ME)

CONTENTS

Revision History

Rev	Date	Modification
1.0	1ST Nov., 2023	Official release

1. Description

DDR5 UDIMM							
Part Number	Density	Data rate	DIMM Organization	Number of DRAM	Number of rank	side	ECC
SQR-UD5N48G5K6ME (Micron 3Gx8(24Gb))	48GB	5600 MT/s	6Gx72	20	2	2	Y

2. Features

- Key Parameter

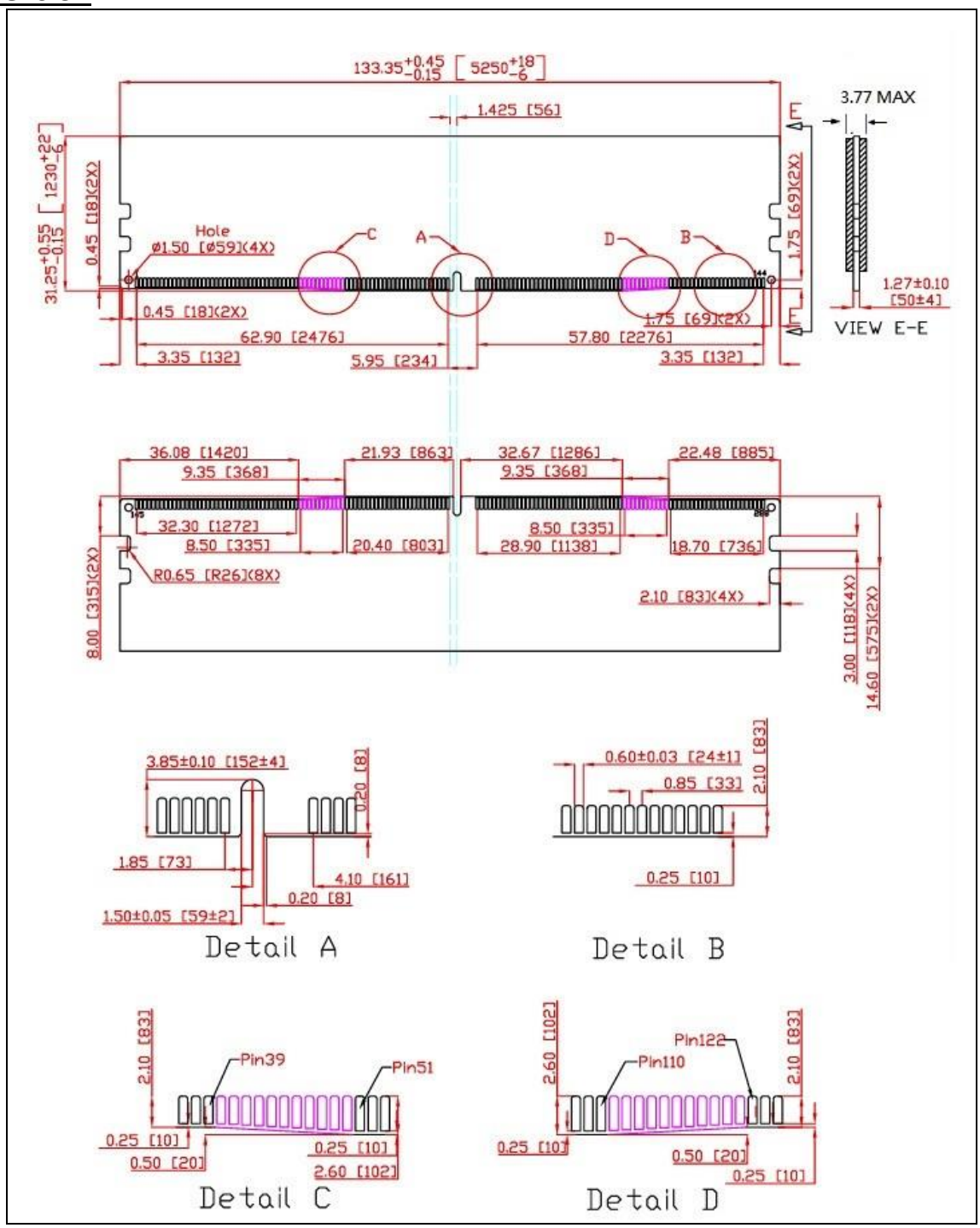
Industry Nomenclature	tCK (ns)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)
PC5-5600	0.357	16.00	16.00	32	48.00

Industry Nomenclature	**Supported Data Transfer Rate**			
	CL=36	**CL=40**	**CL=42**	**CL=46**
PC5-5600	4400	4800	5200	5600

tRFC parameter by IC Configuration					
Parameter	IC Configuration				Unit
	8Gb	16Gb	24Gb	32Gb	
tRFC1,min	195	295	410	410	ns
tRFC2,min	130	160	220	220	ns
tRFCsb,min	115	130	190	190	ns

-
- JEDEC Standard 288-pin Dual In-Line Memory Module
- Cl-tRCD-tRP: 46-45-45
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42,46,50
- Operating Temperature: Tc: 0-95C
  - tREFI 3.9us for 0°C ≤Tcase < 85°C,
  - tREFI 1.95us for 85°C < Tcase ≤ 95°C
- On-Die ECC
- PMIC on DIMM, PMIC on DIMM, VIN_Bulk input supply range: 4.25 V to 5.5 V
- Fly-by topology
- I3C/I2C support
- Terminated control and C/A bus
- SPD EEPROM Hub and Integrated Thermal Sensor
- Halogen-free

3. Dimension



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

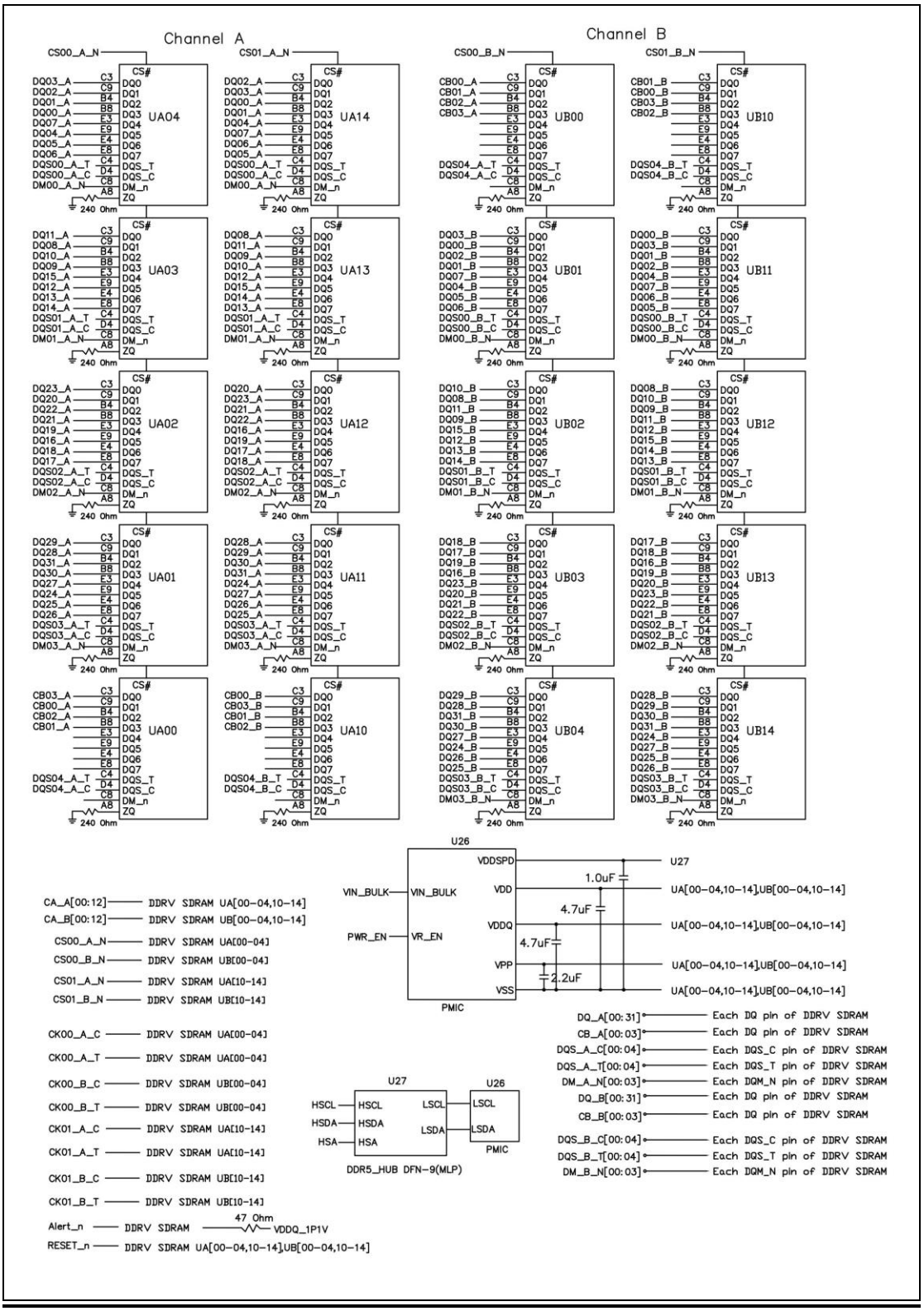
4. Pin Descriptions

Symbol	Type	I/O Level	Description	Symbol	Type	I/O Level	Description
CK_t, CK_c	Input	VDDQ	Clock:	DQ[31:0]_A DQ[31:0]_B	Input/ Output	VDDQ	Data Input/Output
CA[12:0]_A CA[12:0]_B	Input	VDDQ	Command/Address Inputs	CB[3:0]_A CB[3:0]_B	Input/ Output	VDDQ	ECC Check Bits Input/Output
CS[1:0]_A CS[1:0]_B	Input	VDDQ	Chip Select	DQS[4:0]_A_t DQS[4:0]_B_t	Input/ Output	VDDQ	Data Strobe
ALERT_n	Output	VDDQ	Alert	DQS[4:0]_A_c DQS[4:0]_B_c	Input/ Output	VDDQ	Data Strobe
RESET_n	CMOS Input	VDDQ	Active Low Asynchronous Reset	DM[3:0]_A_n DM[3:0]_B_n	Input	VDDQ	Input Data Mask
PWR_GOOD	Input/ Output	VDDQ	Power Good Indicator	VIN_BULK	Supply		External Power Supply
HSCL	Input	VOUT	Host Sideband Bus Clock	PWR_EN	Input		PMIC Enable
HSDA	Input/ Output	VOUT	Host Sideband Bus Data	VSS	Supply		Ground
HAS	Input	GND	Host Sideband Bus Device ID	RFU			Reserved for future use

5. Pin Assignments

288-Pin DDR5 UDIMM Front								288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	DQ20_A	73	CK0_A_c	109	Vss	145	VIN_BULK	181	DQ22_A	217	CK1_A_c	253	Vss
2	RFU	38	Vss	74	Vss	110	DQ5_B	146	VIN_BULK	182	Vss	218	Vss	254	DQ7_B
3	RFU	39	DQ21_A	75	RFU	111	Vss	147	PWR_GOOD	183	DQ23_A	219	RFU	255	Vss
4	HSCL	40	Vss	76	RFU	112	DQ8_B	148	HAS	184	Vss	220	RFU	256	DQ10_B
5	HSDA	41	DQ24_A	77	Vss	113	Vss	149	RFU	185	DQ26_A	221	Vss	257	Vss
6	Vss	42	Vss	78	CK0_B_t	114	DQ9_B	150	Vss	186	Vss	222	CK1_B_t	258	DQ11_B
7	RFU	43	DQ25_A	79	CK0_B_c	115	Vss	151	PWR_EN	187	DQ27_A	223	CK1_B_c	259	Vss
8	Vss	44	Vss	80	Vss	116	DM1_B_n	152	RFU	188	Vss	224	Vss	260	DQS1_B_c
9	DQ0_A	45	DM3_A_n	81	RFU	117	Vss	153	Vss	189	DQS3_A_c	225	RFU	261	DQS1_B_t
10	Vss	46	Vss	82	CA12_B	118	DQ12_B	154	DQ2_A	190	DQS3_A_t	226	RFU	262	Vss
11	DQ1_A	47	DQ28_A	83	Vss	119	Vss	155	Vss	191	Vss	227	Vss	263	DQ14_B
12	Vss	48	Vss	84	CA10_B	120	DQ13_B	156	DQ3_A	192	DQ30_A	228	CA11_B	264	Vss
13	DQS0_A_c	49	DQ29_A	85	CA8_B	121	Vss	157	Vss	193	Vss	229	CA9_B	265	DQ15_B
14	DQS0_A_t	50	Vss	86	Vss	122	DQ16_B	158	DM0_A_n	194	DQ31_A	230	Vss	266	Vss
15	Vss	51	CB0_A	87	CA6_B	123	Vss	159	Vss	195	Vss	231	CA7_B	267	DQ18_B
16	DQ4_A	52	Vss	88	CA4_B	124	DQ17_B	160	DQ6_A	196	CB2_A	232	CA5_B	268	Vss
17	Vss	53	CB1_A	89	Vss	125	Vss	161	Vss	197	Vss	233	Vss	269	DQ19_B
18	DQ5_A	54	Vss	90	CA2_B	126	DQS2_B_c	162	DQ7_A	198	CB3_A	234	CA3_B	270	Vss
19	Vss	55	DQS4_A_c	91	CA0_B	127	DQS2_B_t	163	Vss	199	Vss	235	CA1_B	271	DM2_B_n
20	DQ8_A	56	DQS4_A_t	92	Vss	128	Vss	164	DQ10_A	200	ALERT_n	236	Vss	272	Vss
21	Vss	57	Vss	93	CS0_B_n	129	DQ20_B	165	Vss	201	Vss	237	CS1_B_n	273	DQ22_B
22	DQ9_A	58	CS0_A_n	94	Vss	130	Vss	166	DQ11_A	202	CS1_A_n	238	Vss	274	Vss
23	Vss	59	Vss	95	RESET_n	131	DQ21_B	167	Vss	203	Vss	239	DQS4_B_c	275	DQ23_B
24	DM1_A_n	60	CA0_A	96	Vss	132	Vss	168	DQS1_A_c	204	CA1_A	240	DQS4_B_t	276	Vss
25	Vss	61	CA2_A	97	CB0_B	133	DQ24_B	169	DQS1_A_t	205	CA3_A	241	Vss	277	DQ26_B
26	DQ12_A	62	Vss	98	Vss	134	Vss	170	Vss	206	Vss	242	CB2_B	278	Vss
27	Vss	63	CA4_A	99	CB1_B	135	DQ25_B	171	DQ14_A	207	CA5_A	243	Vss	279	DQ27_B
28	DQ13_A	64	CA6_A	100	Vss	136	Vss	172	Vss	208	CA7_A	244	CB3_B	280	Vss
29	Vss	65	Vss	101	DQ0_B	137	DM3_B_n	173	DQ15_A	209	Vss	245	Vss	281	DQS3_B_c
30	DQ16_A	66	CA8_A	102	Vss	138	Vss	174	Vss	210	CA9_A	246	DQ2_B	282	DQS3_B_t
31	Vss	67	CA10_A	103	DQ1_B	139	DQ28_B	175	DQ18_A	211	CA11_A	247	Vss	283	Vss
32	DQ17_A	68	Vss	104	Vss	140	Vss	176	Vss	212	Vss	248	DQ3_B	284	DQ30_B
33	Vss	69	CA12_A	105	DQS0_B_c	141	DQ29_B	177	DQ19_A	213	RFU	249	Vss	285	Vss
34	DQS2_A_c	70	RFU	106	DQS0_B_t	142	Vss	178	Vss	214	RFU	250	DM0_B_n	286	DQ31_B
35	DQS2_A_t	71	Vss	107	Vss	143	RFU	179	DM2_A_n	215	Vss	251	Vss	287	Vss
36	Vss	72	CK0_A_t	108	DQ4_B	144	RFU	180	Vss	216	CK1_A_t	252	DQ6_B	288	RFU

6. Block Diagram



7. Thermal Characteristics

Symbol	Parameter		Rating	Units	Note
T_c	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2,3
		Extended Temp.	85 to 95	°C	1,2,3,4
T_{STG}	Storage Temperature		-55 to 100	°C	5
HSTG	Non-operating storage relative humidity (non-condensing)		5 to 95	%	

Note:
1. Maximum operating case temperature; Tc is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum Tc during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum Tc during operation.
4. If Tc exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95µs interval refresh rate.
5. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

8. IDD, IDDQ and IPP Specifications

Symbol	Description	Value		Units
		IDD Max.	IPP Max.	
IDD0	Operating One Bank Active-Precharge Current	4450	210	mA
IDD0F	Operating Four Bank Active-Precharge Current	4720	230	mA
IDD2N	Precharge Standby Current	4300	220	mA
IDD2P	Precharge Power-Down Current	4200	160	mA
IDD3N	Active Standby Current	5400	260	mA
IDD3P	Active Power-Down Current	5400	260	mA
IDD4R	Operating Burst Read Current	6450	230	mA
IDD4W	Operating Burst Write Current	6910	510	mA
IDD5B	Burst Refresh Current (Normal Refresh Mode)	6190	460	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	4880	270	mA
IDD6N	Self Refresh Current: Normal Temperature Range	4380	640	mA
IDD6E	Self Refresh Current: Extended Temperature Range	6120	740	mA
IDD7	Operating Bank Interleave Read Current	7450	360	mA
IDD8	Maximum Power Saving Deep Power Down Current	4280	240	mA

The above information may be change due to the update of the device specifications and is for reference only.

9. Timing Parameters

Parameter	Symbol	5600		6000		6400		Unit
		Min	Max	Min	Max	Min	Max	
Clock Timing								
Average clock period	tCK,AVG	0.357		0.333		0.312		ns
Command and Address Timing								
Read to Read command delay for same bank group	tCCD_L	8nCK,5ns (MAX)		8nCK,5ns (MAX)		8nCK,5ns (MAX)		nCK
WRITE to WRITE command delay for same bank group	tCCD_L_WR	32nCK, 20ns (MAX)		32nCK, 20ns (MAX)		32nCK, 20ns (MAX)		nCK
WRITE to WRITE command delay for same bank group, second WRITE not RMW	tCCD_L_WR2	16nCK, 10ns (MAX)		16nCK, 10ns (MAX)		16nCK, 10ns (MAX)		nCK
Read to Read or Write to Write command delay for different bank group for BL16, BC8 OTF	tCCD_S	8		8		8		nCK
ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size	tRRD_S,2K	8		8		8		nCK
ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size	tRRD_S,1K	8		8		8		nCK
ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size	tRRD_L,2K	8nCK,5ns (MAX)		8nCK,5ns (MAX)		8nCK,5ns (MAX)		nCK
ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size	tRRD_L,1K	8nCK,5ns (MAX)		8nCK,5ns (MAX)		8nCK,5ns (MAX)		nCK
Four activate window for 2KB page size	tFAW,2K	40nCK, 14.280ns (MAX)		40nCK, 13.333ns (MAX)		40nCK, 12.500ns (MAX)		ns
Four activate window for 1KB page size	tFAW,1K	32nCK, 11.428ns (MAX)		32nCK, 10.666ns (MAX)		32nCK, 10.000ns (MAX)		ns
Delay from start of internal WRITE transaction to internal READ command for different bank group	tWTR_S	2.5		2.5		2.5		ns
Delay from start of internal WRITE transaction to internal READ command for same bank group	tWTR_L	10		10		10		ns
Delay from start of internal WRITE transaction to internal READ with AUTO PRECHARGE command for same bank	tWTRA	tWR-tRTP		tWR-tRTP		tWR-tRTP		ns
Internal READ command to PRECHARGE command delay	tRTP	7.5		7.5		7.5		ns
PRECHARGE to PRECHARGE delay	tPPD	2		2		2		nCK
WRITE recovery time	tWR	30		30		30		ns

10. SPD

Byte Number	Function Described	Function supported	Hex Value
0	Number of Bytes in SPD Device	1024 Bytes	30
1	SPD Revision for Base Configuration Parameters	Revision 1.0	10
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM	12
3	Key Byte / Module Type	UDIMM	02
4	First SDRAM Density and Package	Monolithic 24Gb	05
5	First SDRAM Addressing	10 columns/17 rows	01
6	First SDRAM I/O Width	x8	20
7	First SDRAM Bank Groups & Banks Per Bank Group	8BGs / 4Banks per BG	62
8	Second SDRAM Density and Package	N/A	00
9	Second SDRAM Addressing	N/A	00
10	Second SDRAM I/O Width	N/A	00
11	Second SDRAM Bank Groups & Banks Per Bank Group	N/A	00
12	SDRAM BL32 & Post Package Repair	BL32 not / sPPR supported / MBIST/mPPR supported	A2
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	PASR supported	12
14	SDRAM Fault Handling	supported	0F
15	Reserved	Reserved	00
16	SDRAM Nominal Voltage, VDD	1.1V	00
17	SDRAM Nominal Voltage, VDDQ	1.1V	00
18	SDRAM Nominal Voltage, VPP	1.8V	00
19	SDRAM Timing	Standard	00
20	SDRAM Minimum Cycle Time (t_{CKAVG}min), Least Significant Byte	357ps	65
21	SDRAM Minimum Cycle Time (t_{CKAVG}min), Most Significant Byte	357ps	01
22	SDRAM Maximum Cycle Time (t_{CKAVG}max), Least Significant Byte	1010ps	F2
23	SDRAM Maximum Cycle Time (t_{CKAVG}max), Most Significant Byte	1010ps	03
24	CAS Latencies Supported, First Byte	22,26,28,30,32,36,40,42,46,50	7A
25	CAS Latencies Supported, Second Byte	22,26,28,30,32,36,40,42,46,50	AD
26	CAS Latencies Supported, Third Byte	22,26,28,30,32,36,40,42,46,50	00
27	CAS Latencies Supported, Fourth Byte	22,26,28,30,32,36,40,42,46,50	00
28	CAS Latencies Supported, Fifth Byte	22,26,28,30,32,36,40,42,46,50	00
29	Reserved	Reserved	00
30	SDRAM Minimum CAS Latency Time (t_{AA}min), Least Significant Byte	16000ps	80
31	SDRAM Minimum CAS Latency Time (t_{AA}min), Most Significant Byte	16000ps	3E
32	SDRAM Minimum RAS to CAS Delay Time (t_{RCD}min), Least Significant Byte	16000ps	80
33	SDRAM Minimum RAS to CAS Delay Time (t_{RCD}min), Most Significant Byte	16000ps	3E
34	SDRAM Minimum Row Precharge Delay Time (t_{RP}min), Least Significant Byte	16000ps	80
35	SDRAM Minimum Row Precharge Delay Time (t_{RP}min), Most Significant Byte	16000ps	3E

36	SDRAM Minimum Active to Precharge Delay Time (t_{RAS}min), Least Significant Byte	32000ps	00
37	SDRAM Minimum Active to Precharge Delay Time (t_{RAS}min), Most Significant Byte	32000ps	7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (t_{RC}min), Least Significant Byte	48000os	80
39	SDRAM Minimum Active to Active/Refresh Delay Time (t_{RC}min), Most Significant Byte	48000os	BB
40	SDRAM Minimum Write Recovery Time (t_{WR}min), Least Significant Byte	30000ps	30
41	SDRAM Minimum Write Recovery Time (t_{WR}min), Most Significant Byte	30000ps	75
42	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC1}min, t_{RFC1}_slr min), Least Significant Byte	410ns	9A
43	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC1}min, t_{RFC1}_slr min), Most Significant Byte	410ns	01
44	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC2}min, t_{RFC2}_slr min), Least Significant Byte	220ns	DC
45	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC2}min, t_{RFC2}_slr min), Most Significant Byte	220ns	00
46	SDRAM Minimum Refresh Recovery Delay Time (t_{RFCsb}min, t_{RFCsb}_slr min), Least Significant Byte	190ns	BE
47	SDRAM Minimum Refresh Recovery Delay Time (t_{RFCsb}_dlr min), Most Significant Byte	190ns	00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC1}_dlr min), Least Significant Byte	N/A	00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC1}_dlr min), Most Significant Byte	N/A	00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC2}_dlr min), Least Significant Byte	N/A	00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC2}_dlr min), Most Significant Byte	N/A	00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFCsb}_dlr min), Least Significant Byte	N/A	00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFCsb}_dlr min), Most Significant Byte	N/A	00
54	SDRAM Refresh Management, First Byte, First SDRAM	N/A	D4
55	SDRAM Refresh Management, Second Byte, First SDRAM	N/A	00
56	SDRAM Refresh Management, First Byte, Second SDRAM	N/A	00
57	SDRAM Refresh Management, Second Byte, Second SDRAM	N/A	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM	N/A	D4
59	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM	N/A	00
60	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM	N/A	00
61	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM	N/A	00
62	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM	N/A	D4
63	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM	N/A	00
64	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM	N/A	00
65	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM	N/A	00
66	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM	N/A	D4
67	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM	N/A	00
68	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM	N/A	00
69	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM	N/A	00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Least Significant Byte	5000ps	88

71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Most Significant Byte	5000ps	13
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Lower Clock Limit	8nCK	08
73	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Least Significant Byte	5000ps	88
74	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Most Significant Byte	5000ps	13
75	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Lower Clock Limit	8nCK	08
76	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Least Significant Byte	20000ps	20
77	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Most Significant Byte	20000ps	4E
78	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Lower Clock Limit	32nCK	20
79	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Least Significant Byte	10000ps	10
80	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Most Significant Byte	10000ps	27
81	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Lower Clock Limit	16nCK	10
82	SDRAM Minimum Four Activate Window (t_{FAW}min), Least Significant Byte	11428ps	A4
83	SDRAM Minimum Four Activate Window (t_{FAW}min), Most Significant Byte	11428ps	2C
84	SDRAM Minimum Four Activate Window (t_{FAW}min), Lower Clock Limit	32nCK	20
85	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Least Significant Byte	10000ps	10
86	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Most Significant Byte	10000ps	27
87	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Lower Clock Limit	16nCK	10
88	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Least Significant Byte	2500ps	C4
89	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Most Significant Byte	2500ps	09
90	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Lower Clock Limit	4nCK	04
91	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Least Significant Byte	7500ps	4C
92	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Most Significant Byte	7500ps	1D
93	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Lower Clock Limit	12nCK	0C
94~127	Reserved -- must be coded as 0x00	Reserved	00
128~191	Reserved for future use	Reserved	00
192	SPD Revision for SPD bytes 192~447	Revision 1.0	10
193	Hashing Sequence	No authentication	00
194	SPD Manufacturer ID Code, First Byte	Montage	86
195	SPD Manufacturer ID Code, Second Byte	Montage	32
196	SPD Device Type	Montage	80
197	SPD Device Revision Number	Montage	15
198	PMIC 0 Manufacturer ID Code, First Byte	Richtek	8A
199	PMIC 0 Manufacturer ID Code, Second Byte	Richtek	8C

200	PMIC 0 Device Type	Richtek	82
201	PMIC 0 Revision Number	Richtek	13
202	PMIC 1 Manufacturer ID Code, First Byte	N/A	00
203	PMIC 1 Manufacturer ID Code, Second Byte	N/A	00
204	PMIC 1 Device Type	N/A	00
205	PMIC 1 Revision Number	N/A	00
206	PMIC 2 Manufacturer ID Code, First Byte	N/A	00
207	PMIC 2 Manufacturer ID Code, Second Byte	N/A	00
208	PMIC 2 Device Type	N/A	00
209	PMIC 2 Revision Number	N/A	00
210	Thermal Sensor Manufacturer ID Code, First Byte	N/A	00
211	Thermal Sensor Manufacturer ID Code, Second Byte	N/A	00
212	Thermal Sensor Device Type	N/A	00
213	Thermal Sensor Revision Number	N/A	00
214	DRAM Specification Level	Reserved	00
215	SPD Specification Level	N/A	00
216	PMIC0 Specification Level	N/A	00
217	PMIC1 Specification Level	N/A	00
218	PMIC2 Specification Level	N/A	00
219	TS Specification Level	N/A	00
220	DIMM Specification Level	N/A	00
221~229	Reserved	Reserved	00
230	Module Nominal Height	31 < height <= 32 mm	11
231	Module Maximum Thickness	1 < thickness <= 2 mm each side	11
232	Reference Raw Card Used	R/C E rev 0	04
233	DIMM Attributes	Tc 0 to +95 °C, 1row	81
234	Module Organization	Symmetrical 2 Package Ranks	08
235	Memory Channel Bus Width	2 channels, 32 bits per channel, ECC	2A
236~239	Reserved	Reserved	00
240~447	Reserved	Reserved	00
448~509	Reserved for future use	Reserved	00
510~511	CRC for SPD bytes 0~509	CRC	17 40
512	Module Manufacturer ID Code, First Byte	Advantech	8A
513	Module Manufacturer ID Code, Second Byte	Advantech	C8
514	Module Manufacturing Location	Made in Taiwan	02
515~516	Module Manufacturing Date		-
517~520	Module Serial Number		-

521~550	Module Part Number	SQR-UD5N48G5K6ME	53 51 52 2D 55 44 35 4E 34 38 47 35 4B 36 4D 45 20 20 20 20 20 20 20 20 20 20 20 20 20
551	Module Revision Code		00
552	DRAM Manufacturer ID Code, First Byte	Micron	80
553	DRAM Manufacturer ID Code, Second Byte	Micron	2C
554	DRAM Stepping		00
555~639	Manufacturer's Specific Data		-
640~703	End User Programmable	Reserved	00
704~767	End User Programmable	Reserved	00
768~831	End User Programmable	Reserved	00
832~895	End User Programmable	Reserved	00
896~959	End User Programmable	Reserved	00
960~1023	End User Programmable	Reserved	00

Appendix: Part Number Table

Product	Advantech PN
SQRAM 48GB ECC U-DDR5-5600 3Gx8 Micron (0~95)	**SQR-UD5N48G5K6ME**